WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a first semiconductor region formed in a surface region of a semiconductor substrate;

a second semiconductor region formed separately from said first semiconductor region in said surface region of said semiconductor substrate;

a gate insulating film formed on a portion of said semiconductor substrate which is arranged between said first and second semiconductor regions;

a gate electrode formed on said gate insulating film;

an interlayer insulating film formed on said semiconductor substrate to cover said first semiconductor region, second semiconductor region and gate electrode;

first and second lower electrodes formed on said interlayer insulating film;

a first contact plug formed in said interlayer insulating film in contact with said first lower electrode;

a second contact plug formed separately from said first contact plug and in contact with said second lower electrode in said interlayer insulating film;

a first ferroelectric film formed on said first lower electrode;

a first upper electrode formed on said first

ferroelectric film;

a second ferroelectric film formed on said second lower electrode; and

a second upper electrode formed on said second ferroelectric film.

2. The semiconductor device according to claim 1, wherein said first and second lower electrodes are separately formed.

3. The semiconductor device according to claim 1, wherein said first and second lower electrodes are integrally formed.

4. The semiconductor device according to claim 3, wherein said first and second ferroelectric films are integrally formed.

5. The semiconductor device according to claim 1, wherein said first and second contact plugs are integrally formed in a portion of said interlayer insulating film which lies between said first semiconductor region and said first and second lower electrodes and the integrally formed contact plugs are formed in contact with said first semiconductor region.

6. The semiconductor device according to claim 1, wherein said first upper electrode is connected to said second semiconductor region.

7. The semiconductor device according to claim 1, wherein said first lower electrode, first ferroelectric film and first upper electrode are combined to

configure a first ferroelectric capacitor and said second lower electrode, second ferroelectric film and second upper electrode are combined to configure a second ferroelectric capacitor

8. The semiconductor device according to claim 7, wherein said first semiconductor region is a source, said second semiconductor region is a drain and said gate electrode, source, drain and semiconductor substrate are combined to configure a cell transistor.

9. The semiconductor device according to claim 8, wherein a series connected TC unit type ferroelectric memory comprises series connected memory cells each having said cell transistor (T) having said source and said drain and said first ferroelectric capacitor (C) inbetween said source and said drain.

10. A semiconductor device comprising:

a first semiconductor region formed in a surface region of a semiconductor substrate;

a second semiconductor region formed separately from said first semiconductor region in said surface region of said semiconductor substrate;

a gate insulating film formed on a portion of said semiconductor substrate which is arranged between said first and second semiconductor regions;

a gate electrode formed on said gate insulating film;

an interlayer insulating film formed on said

semiconductor substrate to cover said first semiconductor region, second semiconductor region and gate electrode;

first and second lower electrodes formed on said interlayer insulating film;

a contact plug formed in a portion of said interlayer insulating film which is arranged between said first semiconductor region and said first and second lower electrodes;

a first ferroelectric film formed on said first lower electrode;

a first upper electrode formed on said first ferroelectric film;

a second ferroelectric film formed on said second lower electrode; and

a second upper electrode formed on said second ferroelectric film.

11. The semiconductor device according to claim 10, wherein said first and second lower electrodes are separately formed.

12. The semiconductor device according to claim 10, wherein said first and second lower electrodes are integrally formed.

13. The semiconductor device according to claim 12, wherein said first and second ferroelectric films are integrally formed.

14. The semiconductor device according to

claim 10, wherein said contact plug is formed to partly overlap a portion above said gate electrode.

15. The semiconductor device according to claim 10, wherein said first upper electrode is connected to said second semiconductor region.

16. The semiconductor device according to claim 10, wherein said first lower electrode, first ferroelectric film and first upper electrode are combined to configure a first ferroelectric capacitor and said second lower electrode, second ferroelectric film and second upper electrode are combined to configure a second ferroelectric capacitor

17. The semiconductor device according to claim 16, wherein said first semiconductor region is a source, said second semiconductor region is a drain and said gate electrode, source, drain and semiconductor substrate are combined to configure a cell transistor.

18. The semiconductor device according to claim 17, wherein a series connected TC unit type ferroelectric memory comprises series connected memory cells each having said cell transistor (T) having said source and said drain and said first ferroelectric capacitor (C) inbetween said source and said drain.

19. A semiconductor device comprising:

first semiconductor regions formed in a surface region of a semiconductor substrate;

second semiconductor regions formed separately

from said first semiconductor regions in said surface region of said semiconductor substrate;

gate insulating films respectively formed on portions of said semiconductor substrate which is arranged between said first semiconductor regions and said second semiconductor regions;

gate electrodes respectively formed on said gate insulating films;

an interlayer insulating film formed on said semiconductor substrate to cover said first semiconductor regions, second semiconductor regions and gate electrodes;

first lower electrodes formed on said interlayer insulating film;

second lower electrodes formed separately from said first lower electrodes on said interlayer insulating film;

contact plugs formed in portions of said interlayer insulating film which lie between said first semiconductor regions and said first and second lower electrodes;

first ferroelectric films respectively formed on said first lower electrodes;

first upper electrodes respectively formed on said first ferroelectric films;

second ferroelectric films respectively formed on said second lower electrodes; and

second upper electrodes respectively formed on said second ferroelectric films.

20. The semiconductor device according to claim 19, wherein a width of a cross section of said contact plug in an array direction of said gate electrodes is larger than a distance between said gate electrodes which are arranged on both sides of said first semiconductor region.

21. The semiconductor device according to claim 20, wherein said contact plug is formed in a self-alignment process by using two gate electrodes arranged on both sides of said first semiconductor region as a mask and said contact plug partly overlaps portions above said two gate electrodes.

22. A semiconductor device manufacturing method comprising:

forming a gate electrode over a semiconductor substrate with a gate insulating film interposed between said semiconductor substrate and said gate electrode;

forming source and drain diffusion layers on a surface of said semiconductor substrate on both sides of said gate electrode;

forming a first interlayer insulating film on said semiconductor substrate to cover said gate electrode, source and drain diffusion layers;

forming a buried interconnection and a first

contact plug which extends from a portion of said buried interconnection to one of said source diffusion layer and said drain diffusion layer in said first interlayer insulating film which lies on one of said source diffusion layer and said drain diffusion layer;

forming a second interlayer insulating film on said first interlayer insulating film and on said buried interconnection containing said first contact plug;

forming a pair of second and third contact plugs which extend from a surface of said second interlayer insulating film to said buried interconnection in said second interlayer insulating film formed on said buried interconnection; and

forming a first ferroelectric capacitor by sequentially laminating a first lower electrode, first ferroelectric film and first upper electrode in this order on said second contact plug and forming a second ferroelectric capacitor by sequentially laminating a second lower electrode, second ferroelectric film and second upper electrode in this order on said third contact plug.

23. The semiconductor device manufacturing method according to claim 22, wherein said first and second lower electrodes are integrally formed, said first and second ferroelectric films are separately formed and said first and second upper electrodes are separately

formed.

24. The semiconductor device manufacturing method according to claim 22, wherein said first and second lower electrodes are integrally formed, said first and second ferroelectric films are integrally formed and said first and second upper electrodes are separately formed.